REMARKS

Claims 20, 22-33, and 35-42 were pending in the present application. Claim 22 has been amended. Accordingly, claims 20, 22-33, and 35-42 remain pending in the application.

Claim 22 is objected to for informalities. Claim 22 has been amended to correct the error.

Rejections under 35 U.S.C. §112, 1st paragraph

"non-reconfigurable host processor"

The Examiner rejected claims 20, 33, and 40 for lack of written description, based on the inclusion of the phrase "non-reconfigurable host" in those claims. Applicant respectfully traverses these rejections.

Applicant submits that even though the specification does not explicitly use the phrase "non-reconfigurable host processor," one of ordinary skill in the art would recognize that an embodiment of a non-reconfigurable host processor is disclosed in the specification, and thus that the inventor had possession of this feature of the claim. The specification states at the outset that "[t]raditionally, the host processor choice is *fixed*" "and code to be executed by the host processor is compiled specific to the processor." *Id.* at [0004] (emphasis added). Then consider host processor 148 shown in Fig. 1. While host processor 148 is not explicitly labeled as "non-reconfigurable," the specification juxtaposes its description of host processor 148 with "*reconfigurable* processor core 150." *See* specification at [0004], [0014]. By not denoting that host processor 148 is reconfigurable and noting that core 150 is "reconfigurable," one of ordinary skill in the art would understand that host processor 148 represents an embodiment of "non-reconfigurable," particularly in view of the description of paragraph [0004]. Accordingly, the specification discloses adding a reconfigurable processor core to the traditional "fixed" host processor choice. Applicant submits that at least these passages

provide ample support for the phrase "non-reconfigurable host processor." Applicant therefore requests removal of this rejection.

"wherein the second portion of the plurality of processors is coupled to memory locations storing instructions executable by the second portion to implement a set of host processor functionality that includes controlling portions of the reconfigurable processor core and interfacing with a system external to the wireless communication device"

The Examiner rejected claims 20 and 40 for lack of written description, based on the phrase "wherein the second portion of the plurality of processors is coupled to memory locations storing instructions executable by the second portion to implement a set of host processor functionality that includes controlling portions of the reconfigurable processor core and interfacing with a system external to the wireless communication device." Applicant respectfully traverses these rejections.

Applicant submits the specification [0014] discloses that embodiments of core 150 can include at least two different types of processors (e.g., ARM, MIPS, DSP), one of which can be different from the host processor 148. *See* specification at [0014]. In addition, Applicant submits it is well known to those of ordinary skill in the art that processors process instructions. The specification alludes to this, noting that a portion of core 150 and host processor 148 can process instructions belonging to different processor families. *Id.* It is also well known to those of ordinary skill in the art that instructions executed by processors can be stored in memory. The specification specifically states this, referring to an "exemplary" processor in core 150 using a program counter (PC) to address instructions within memory system 170. *Id.* at [0015]. The specification therefore clearly discloses embodiments that provide support for the "second portion of the plurality of processors is coupled to memory locations storing instructions executable by the second portion to implement a set of host processor functionality" as in claims 20 and 40.

Applicant submits the specification discloses embodiments that support that host processors "coordinate[] the central processing units and interface[] with an external system." *Id.* at [0002]. Thus, it is therefore apparent to one of ordinary skill in the art that the specification discloses embodiments of "… a set of host processor functionality that includes controlling portions of the reconfigurable processor core and interfacing with a system external to the wireless communication device" as recited in claim 20 and similarly, in claim 40.

Thus, Applicant respectfully submits the above phrase is supported, and Applicant requests the Examiner withdraw the rejection.

"processor type select circuit"

The Examiner rejected claims 20, 33, and 40 for lacking written description based on the phrase "a processor type select circuit configured to select either the non-reconfigurable host processor or the second portion of the plurality of processors to implement the set of host processor functionality." Applicant respectfully traverses these rejections.

The specification discloses (emphasis added):

> In one aspect, an integrated circuit capable of supporting a plurality of host processor families includes a host processor belonging to a first processor family; a reconfigurable processor core coupled to the host processor, the reconfigurable processor core having a core portion processing instructions belonging to a second host processor family; and a processor type select circuit *to configure the integrated circuit to process instructions* belonging to one of the first *or* second host processor family instruction set.

See specification at [0004]. As the Examiner notes, the specification discloses embodiments having "a processor type select circuit to configure the integrated circuit to process instructions belonging to one of the first or second host processor family instruction set." *See* specification at [0004]. That same paragraph makes clear that the "host processor belong[s] to a first processor family" and that the "reconfigurable

processor core" has "a core portion processing instructions belonging to a second host processor family." *Id.* Thus, it would be clear to one of ordinary skill in the art that an embodiment of the select circuit is "select[ing] either the non-reconfigurable host processor or the second portion of the plurality of processors to implement the set of host processor functionality" as recited in claim 20, as well as claims 33 and 40. Thus, Applicant respectfully requests the Examiner remove this rejection.

Rejection under 35 U.S.C. §103

Claims 20, 22-33, and 35-42 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Schmidt (U.S. Patent No. 7,142,882) in view of Applicant Admitted Prior Art (APA). Applicant respectfully traverses this rejection. Applicant maintains arguments made in previous responses dated January 17, 2008, and June 16, 2008 to preserve them for appeal. Applicant has added additional arguments to further highlight why the claims patentably distinguish over the cited art.

Applicant's claim 20 recites a wireless communication device comprising:

> a single integrated circuit die including:
> a reconfigurable processor core including a plurality of processors, wherein a first portion of the plurality of processors is configured to execute instructions belonging to an instruction set of a first processor family and wherein a second portion of the plurality of processors is configured to execute instructions belonging to an instruction set of a second processor family, wherein the second portion of the plurality of processors is coupled to memory locations storing instructions executable by the second portion to implement a set of host processor functionality that includes controlling portions of the reconfigurable processor core and interfacing with a system external to the wireless communication device;
> a non-reconfigurable host processor coupled to the reconfigurable processor core and configured to execute instructions belonging to an instruction set of a first processor family, wherein the non-reconfigurable host processor is coupled to memory locations storing instructions executable by the non-reconfigurable host processor to implement the set of host processor functionality; and
> a processor type select circuit configured to select either the non-reconfigurable host processor or the second portion of the plurality

> of processors to implement the set of host processor functionality. (Emphasis added)

The Examiner asserts Schmidt teaches all of the limitations recited in claim 20, with the exception of the recited "processor" being a host processor, which the Examiner asserts is taught in the APA. As described in the previous response to Office action, dated January 17, 2008, Applicant submits the following paragraph is not found in Schmidt and is found in the specification of Applicant's instant application:

> Moreover, a portion of the reconfigurable processor core **150** can be organized as a second host processor processing instructions belonging to a second host processor family, while the host processor **148** belongs to a first processor family that processes instructions belonging to the first host processor family instruction set. In one embodiment, the host processor **148** is MIPS compatible, while the second host processor portion of the processor core **150** can be ARM compatible. (*See* page 7, lines 13-18) (Emphasis added)

Applicant submits that neither the background section (the APA, according to the Examiner) nor Schmidt teaches or suggests having a "non-reconfigurable host processor" "execute instructions belonging to an instruction set of a first processor family" and a second portion of the processors of the reconfigurable core that "executes instructions belonging to an instruction set of a second processor family" (i.e., "instructions executable by the second portion to implement a set of host processor functionality that control[s] portions of the reconfigurable processor core and interfac[es] with a system external to the wireless communication device" as in claim 20) using a second instruction set. Similarly, the cited references do not teach or suggest a processor type circuit that "select[s] either" the host processor or the second portion of the reconfigurable processor core to "implement the host processor functionality," as recited in claim 20.

In addition, claim 20 recites that the host processor is "non-reconfigurable" and is coupled to the reconfigurable core. As such, the "host processor" of claim 20 cannot, by the terms of the claim, be one of the processors within Schmidt's processor core 150, as suggested by the Examiner in the rejection of claim 20.

Furthermore, the Examiner asserts "it would have been obvious" "to implement a host processor in order to improve the performance and to take advantage of commercially available off the shelf systems." *See* Office action dated October 30, 2008 at page 3. Applicant disagrees with the Examiner's assertion. Specifically, in *KSR*, the Court quoted *In re Kahn* and stated that "[r]ejections on obviousness cannot be satisfied by mere conclusory statements instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *See* 72 Fed. Reg. 57526, 57528-57529, "Examination Guidelines for Determining Obviousness Under 35 U.S.C. 103 in View of the Supreme Court Decision in *KSR International Co. v. Teleflex Inc.*" (Oct. 10, 2007).

Applicant submits the Examiner has merely pointed out that it would be obvious to implement a host processor to improve performance and take advantage of commercially off the shelf systems. The Examiner has not shown rationales such as, for example, "use of a known technique to improve similar devices in the same way," or "applying a known technique to a known device ready for improvement to yield predictable results." *Id.* at 57529.

Applicant notes that neither the APA nor Schmidt discloses "a processor type select circuit," which is required to select "either the non-reconfigurable host processor or the second portion of the plurality of processors" to "implement the set of host processor functionality." In addition, neither the APA nor Schmidt discloses "a first portion of the plurality of processors is configured to execute instructions belonging to an instruction set of a first processor family and wherein a second portion of the plurality of processors is configured to execute instructions belonging to an instruction set of a second processor family." Accordingly, Applicant submits that one skilled in the art would not have a reason to implement a host processor on the same integrated circuit as the reconfigurable core, since doing so would not in and of itself readily improve performance.

Accordingly, Applicant submits none of the cited references teach or disclose the combination of features recited in Applicant's claim 20. Thus, Applicant submits claim 20 and its dependent claims patentably distinguish over the cited references for at least the reasons given above.

Applicant's claims 33 and 40 include features that are similar to the features recited in claim 20. Accordingly, for at least the reasons given above, Applicant submits claims 33 and 40, along with their respective dependent claims patentably distinguish over the cited references.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any extension of time (under 37 C.F.R. § 1.136) is necessary to prevent the above-referenced application from becoming abandoned, Applicant hereby petitions for such extension.

The Commissioner is authorized to charge any fees that may be required, or credit any overpayment, to Meyertons, Hood, Kivlin, Kowert & Goetzel, P.C. Deposit Account No. 501505/6057-61200/SJC.

Respectfully submitted,

Date: December 22, 2008

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